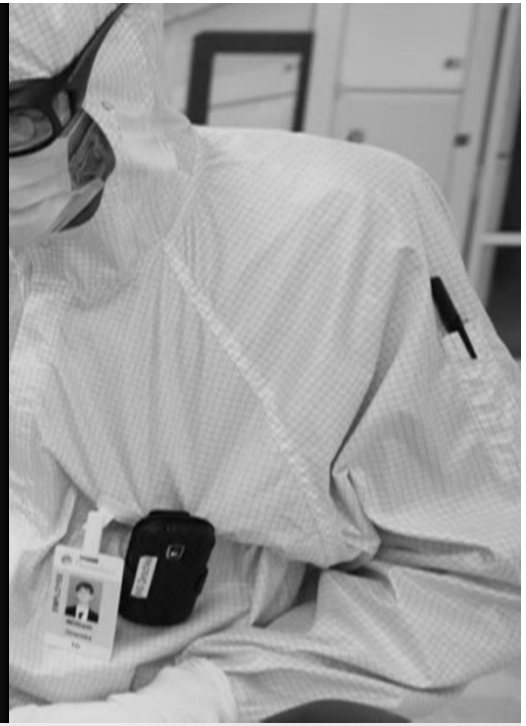

External Cleanup PLL Closed Loop Stability Analysis and Phase Noise consideration

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Summery of Analysis

- This analysis is based on external (board) clean up PLL used with HSS Cores.
- Use of clean up PLL allows for utilizing less expensive oscillator and lower Reference frequencies. It also greatly helps to clean recovered clock phase noise from receiver (Rx).
- The overall closed loop system peaking (Generally three PLLs chained) may require less than 0.1 dB peaking.
- Closed loop analysis of system need to show good stability. **65 degree or better *Phase Margin*** and acceptable ***Gain Margin .***
- PLL in HSS core can contribute ***peaking*** to overall closed loop system. Generally clean up PLL shows good capability of jitter clean up due to its close loop low bandwidth (i.e. Khz range).

Summery of Analysis Continued….

- Pole/Zero approximation of three PLLs chained using Matlab RF tool box shows very good correlation to hardware measurements. “rationalfit” function of RF tool box, allows for representation of low entropy transfer function.

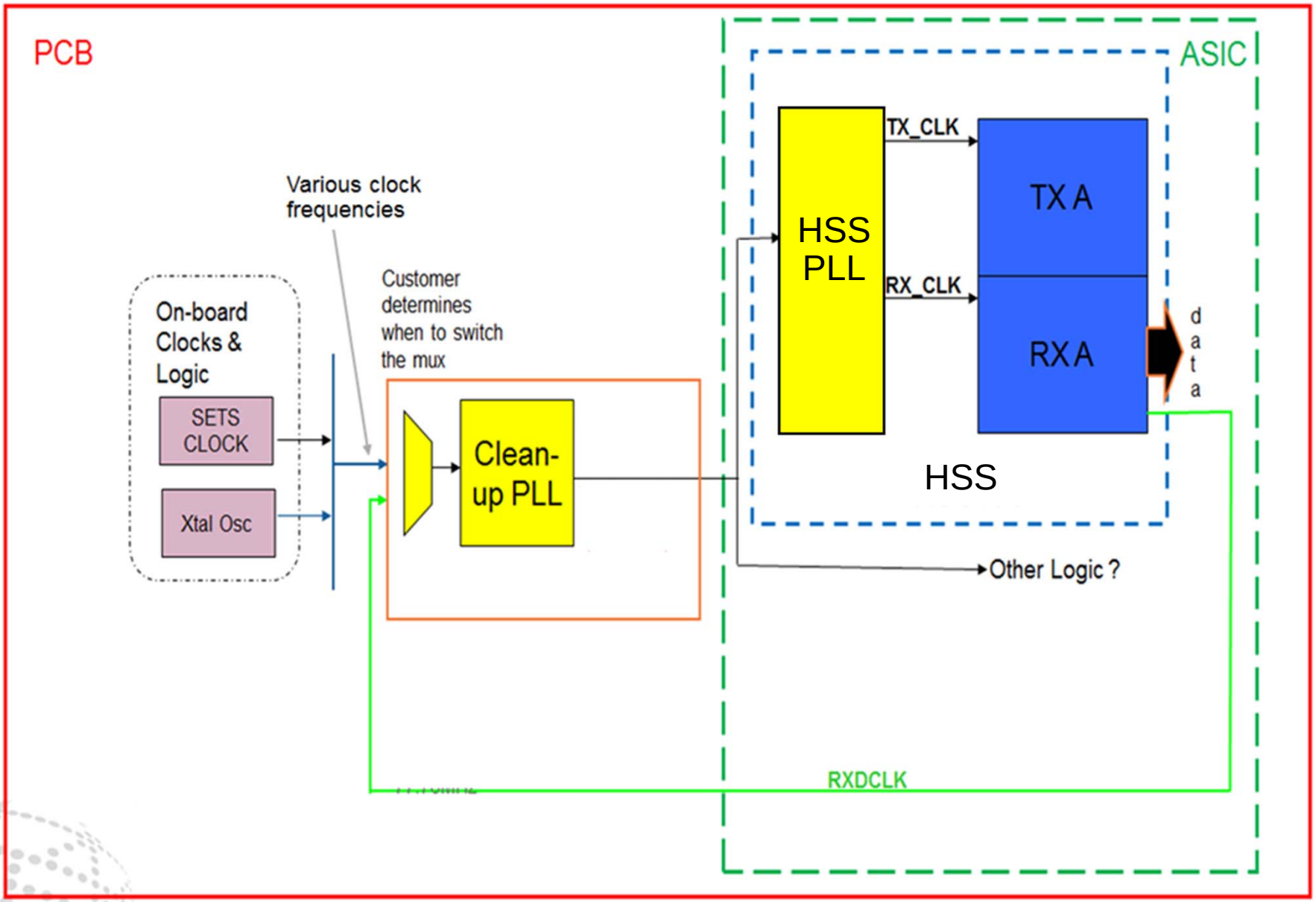
- Possible large signal (Time domain) simulation of closed loop system can be designed in combination of using Simulink and its communication tool box.

- Location and values of Poles and Zeros of the closed loop plotted and calculated. Location of Poles & Zeros in left half side of imaginary axis can further enhance understanding of dominant Poles & Zeros.

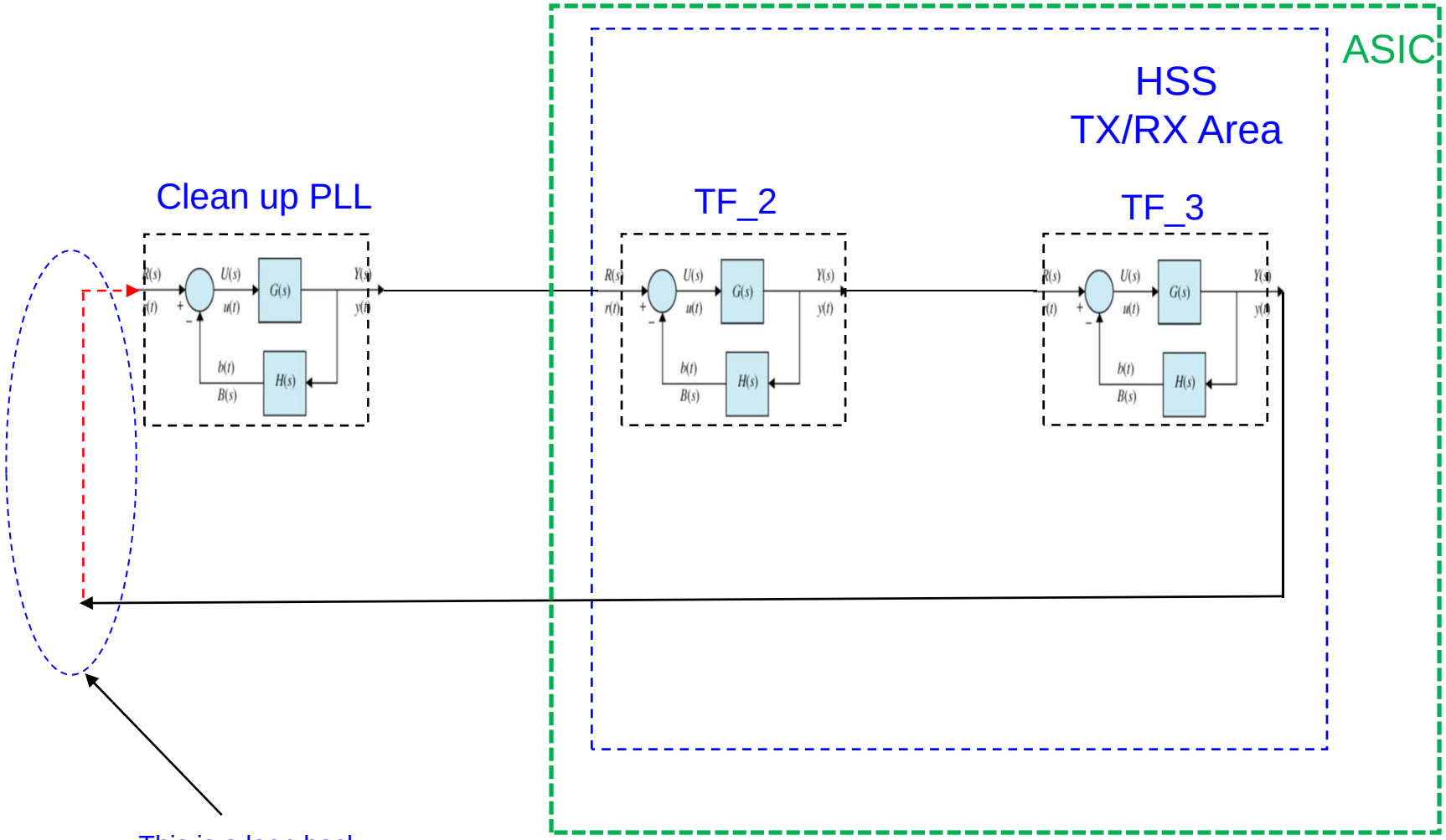
- Phase noise analysis of recovered clock from HSS receiver, also discussed using utilizing Matlab programming.

- Matlab/Simulink interface with software products from independent, third-party services used in this analysis.

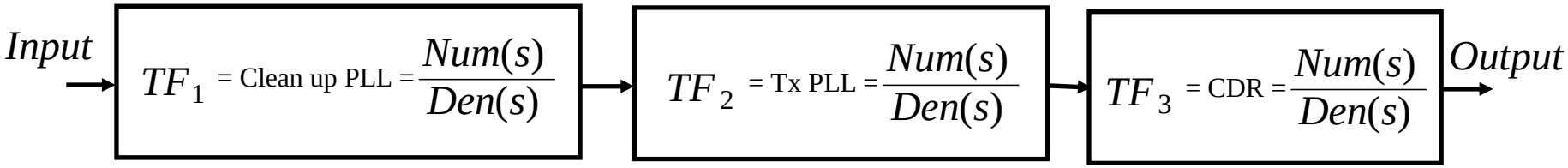
High-level System Design Example for External Clean up PLL



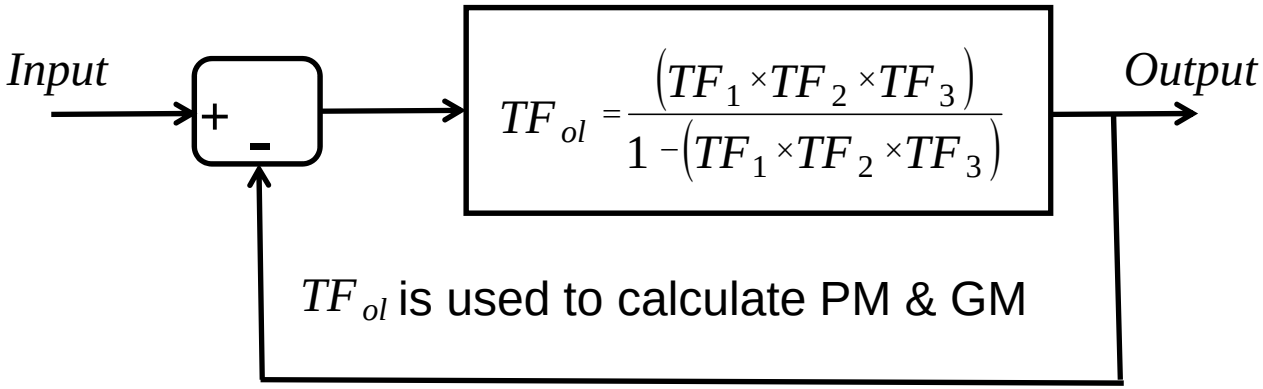
PCB


ASIC
HSS
TX/RX Area
Clean up PLL
TF_2
TF_3
R(s)
U(s)
G(s)
Y(s)
r(t)
u(t)
y(t)
b(t)
B(s)
H(s)
This is a loop back at PCB for this analysis

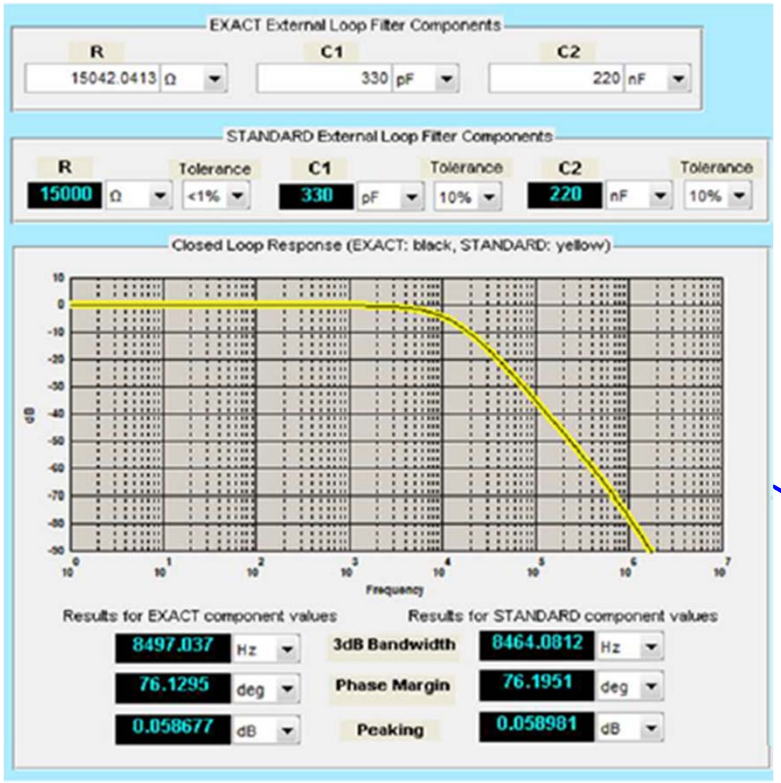
- Clean up PLL transfer function TF_1 synthesized in S-domain.
- Tx PLL transfer function TF_2 synthesized in S-domain.
- RX/CDR transfer function TF_3 synthesized in S-domain.

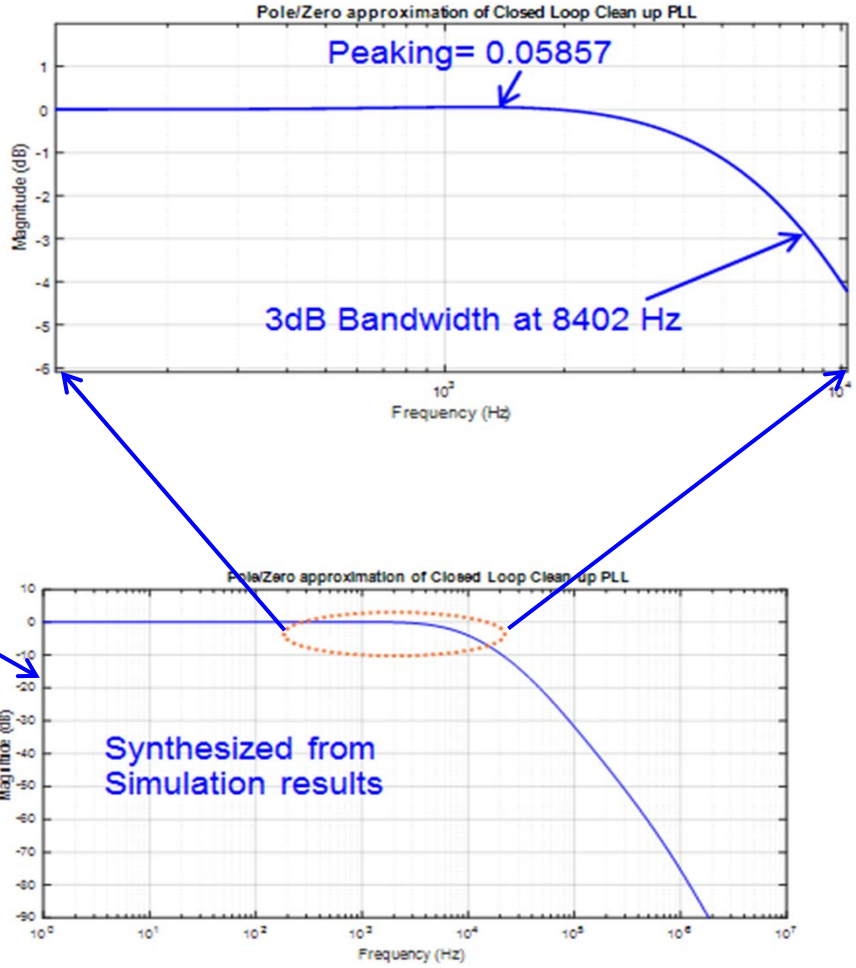


$$\frac{Output}{Input} = TF = TF_1 \times TF_2 \times TF_3$$



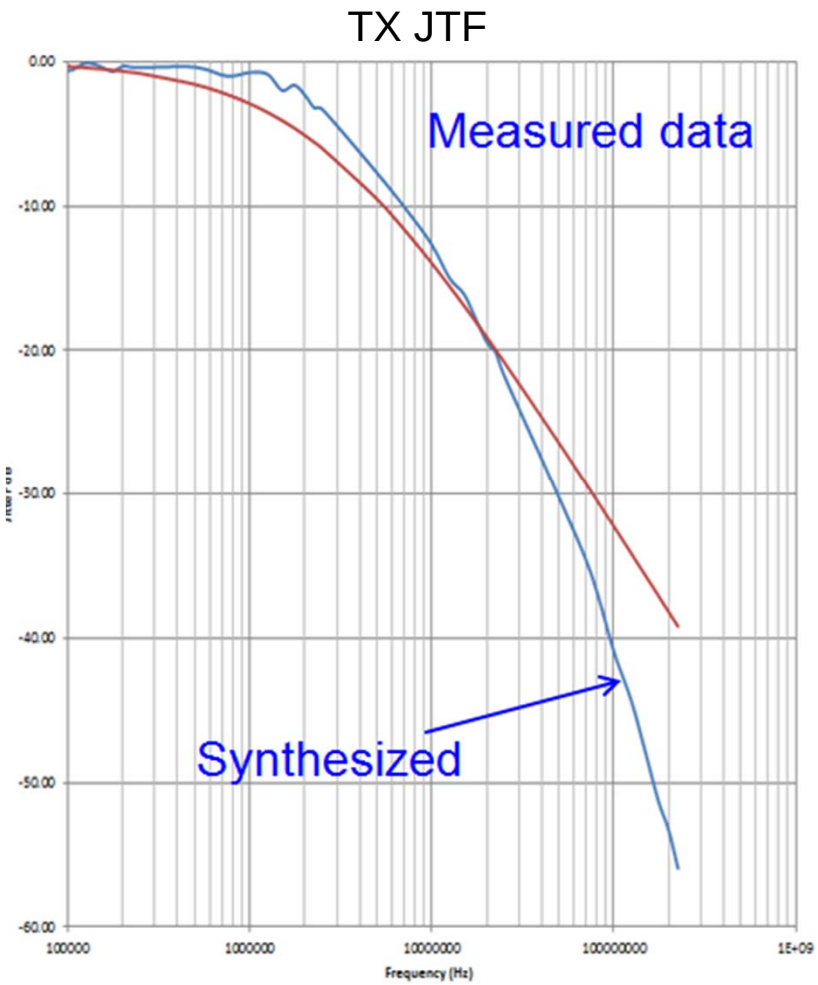
Synthesizing clean up PLL closed loop bandwidth

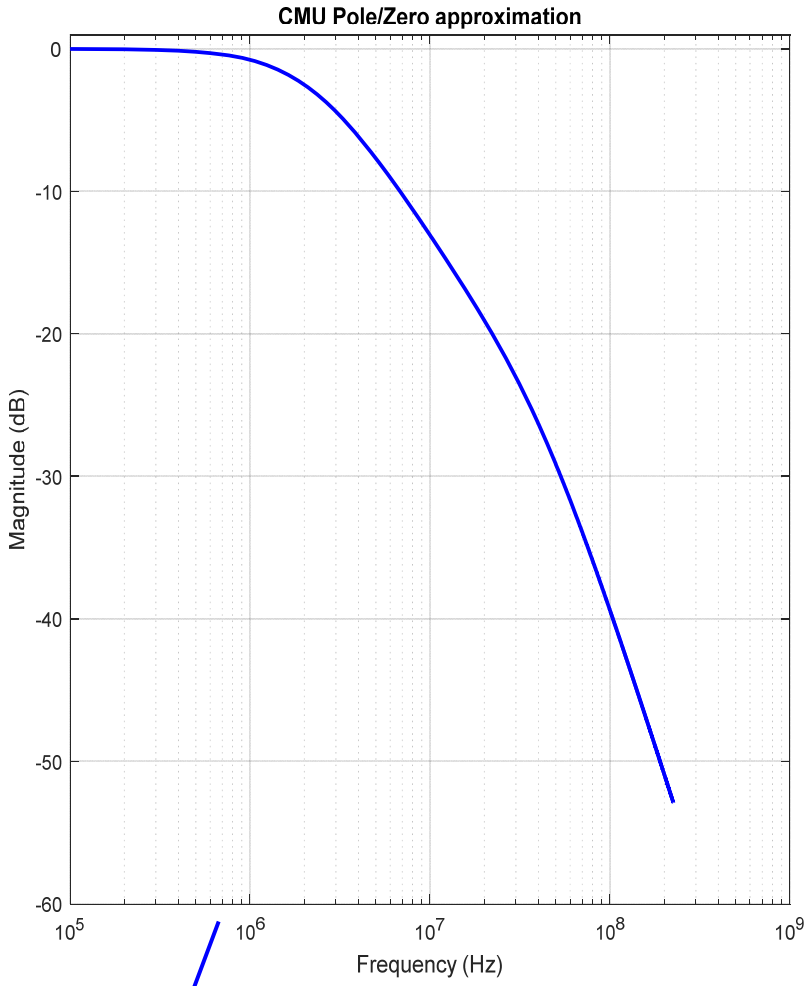




$$TF_{cleanup\_pll} = \frac{(5.39e16)s + 4.933e20}{s^4 + (5.262e6)s^3 + (1.325e12)s^2 + (6.367e16)s + 4.933e20}$$

Synthesizing Tx JTF



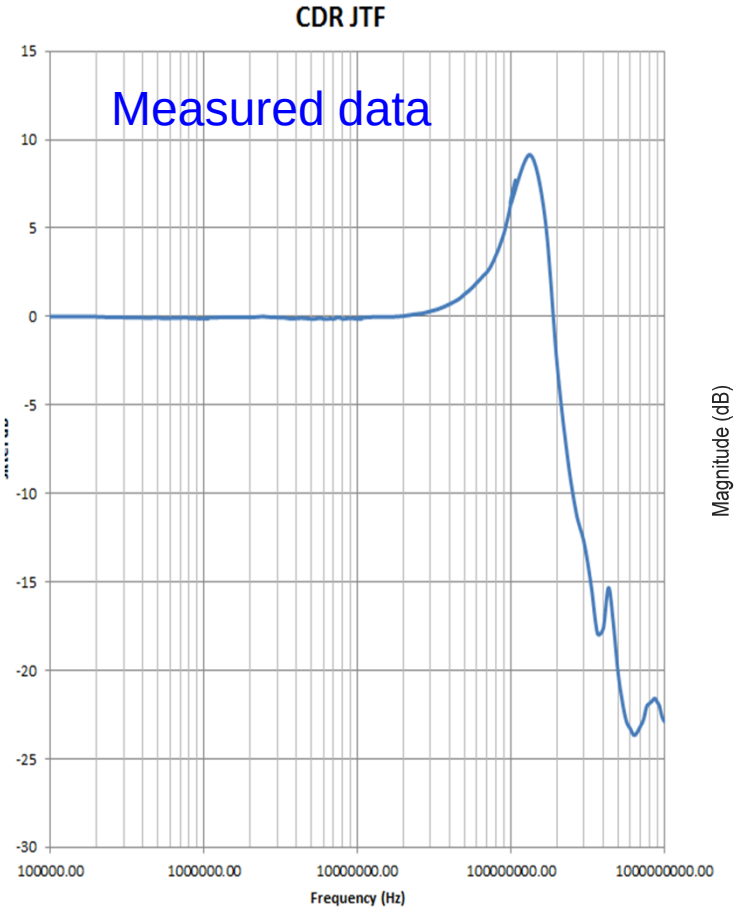


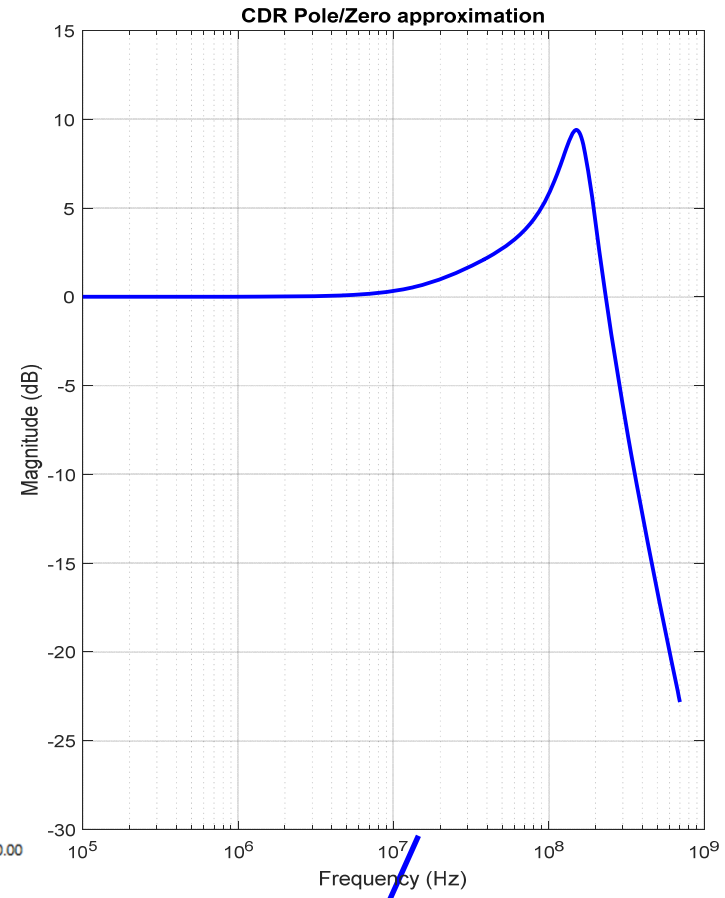
Poles:
-2.2997e8
-1.9783e8
-14.202e6

Zero:
-140e6

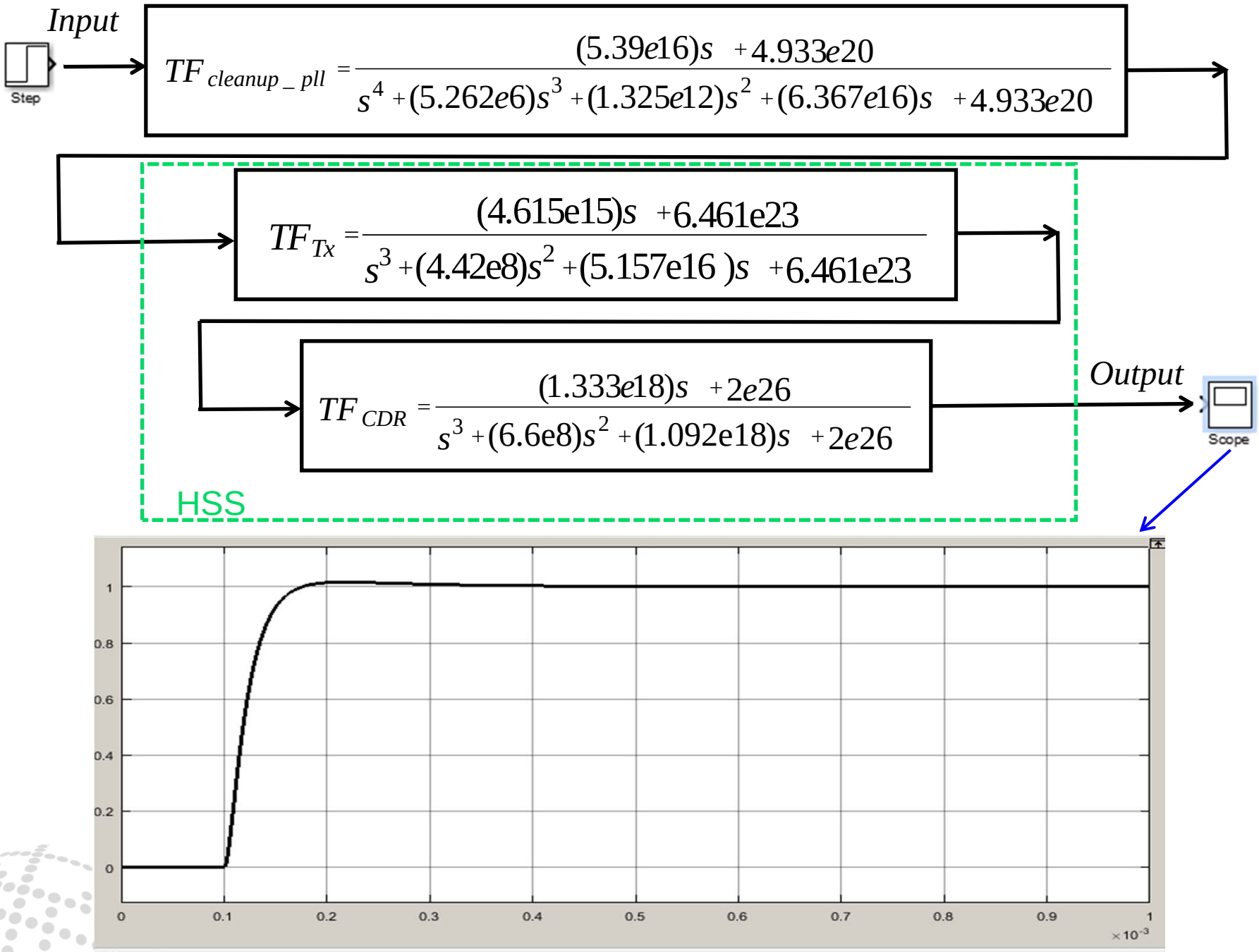
$$TF_{Tx} = \frac{(4.615e15)s + 6.461e23}{s^3 + (4.42e8)s^2 + (5.157e16)s + 6.461e23}$$

Synthesizing CDR JTF

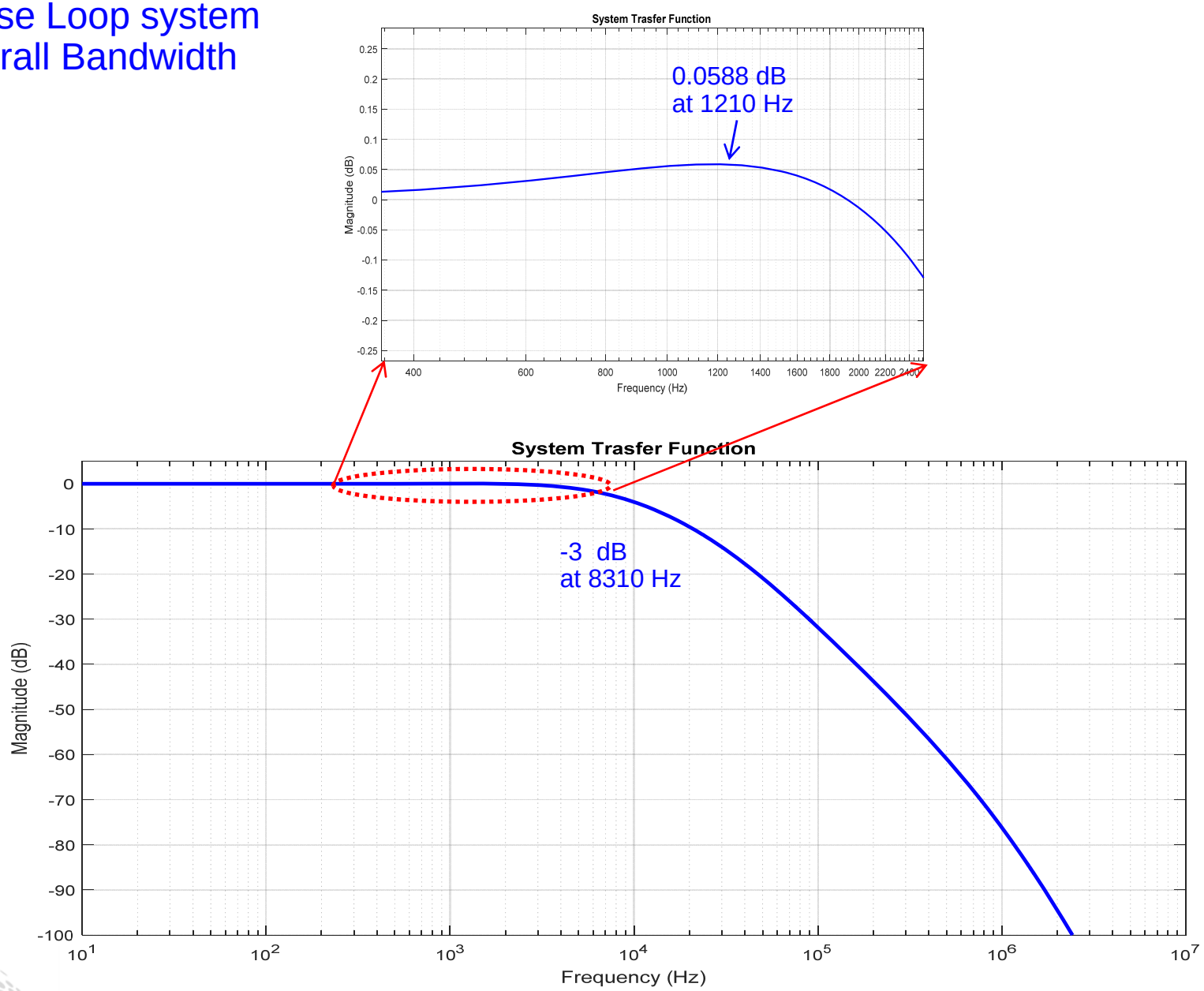




$$TF_{CDR} = \frac{(1.333e18)s + 2e26}{s^3 + (6.6e8)s^2 + (1.092e18)s + 2e26}$$


Input
Step
$TF_{cleanup\_pll} = \frac{(5.39e16)s + 4.933e20}{s^4 + (5.262e6)s^3 + (1.325e12)s^2 + (6.367e16)s + 4.933e20}$
$TF_{Tx} = \frac{(4.615e15)s + 6.461e23}{s^3 + (4.42e8)s^2 + (5.157e16)s + 6.461e23}$
$TF_{CDR} = \frac{(1.333e18)s + 2e26}{s^3 + (6.6e8)s^2 + (1.092e18)s + 2e26}$
Output
Scope
HSS
1
0.8
0.6
0.4
0.2
0
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
×10^-3

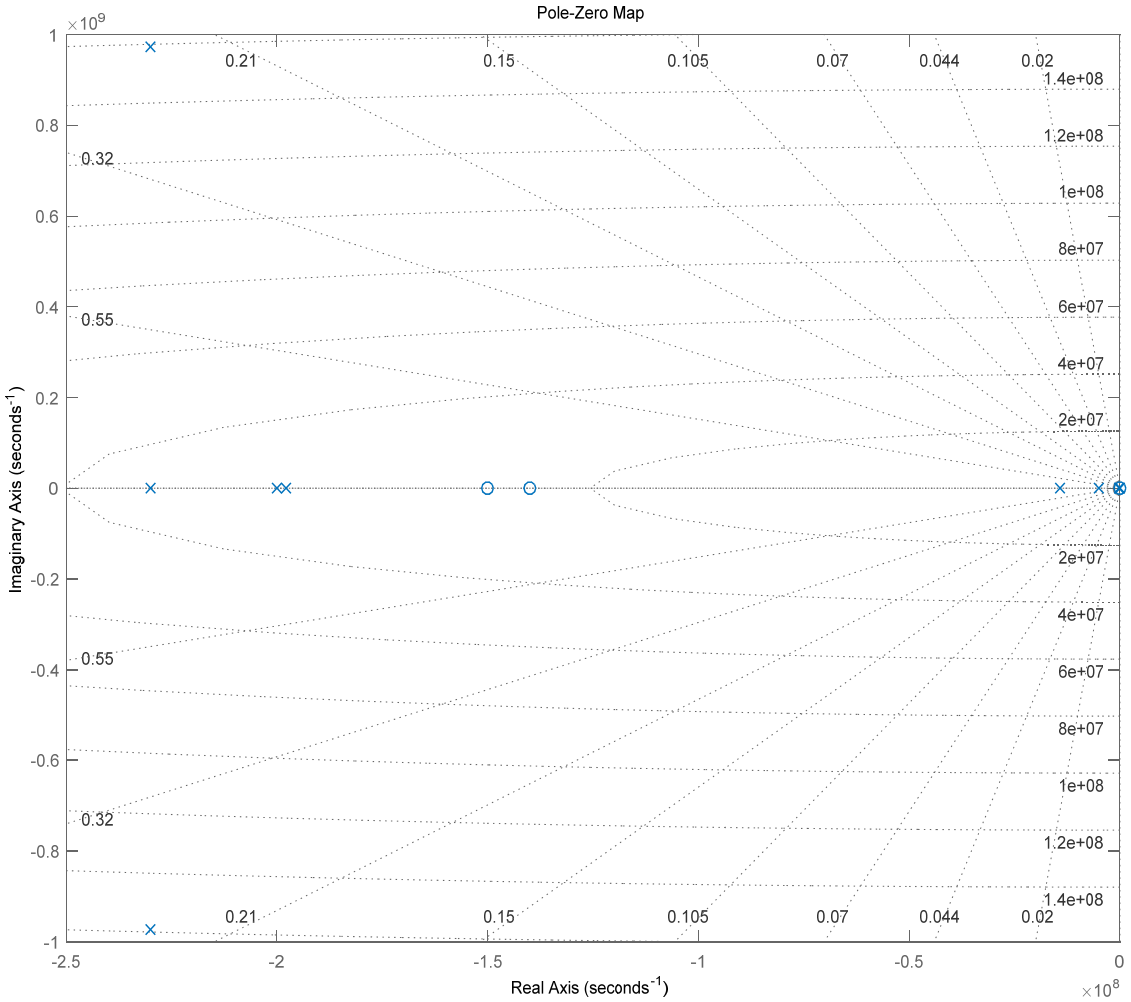
Close Loop system overall Bandwidth

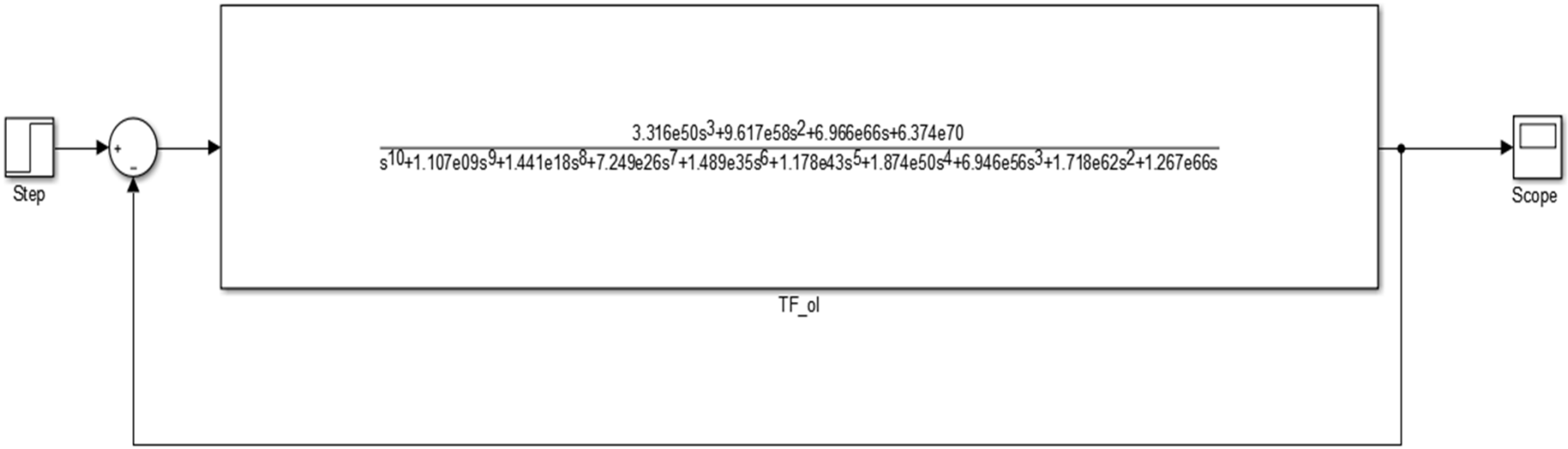


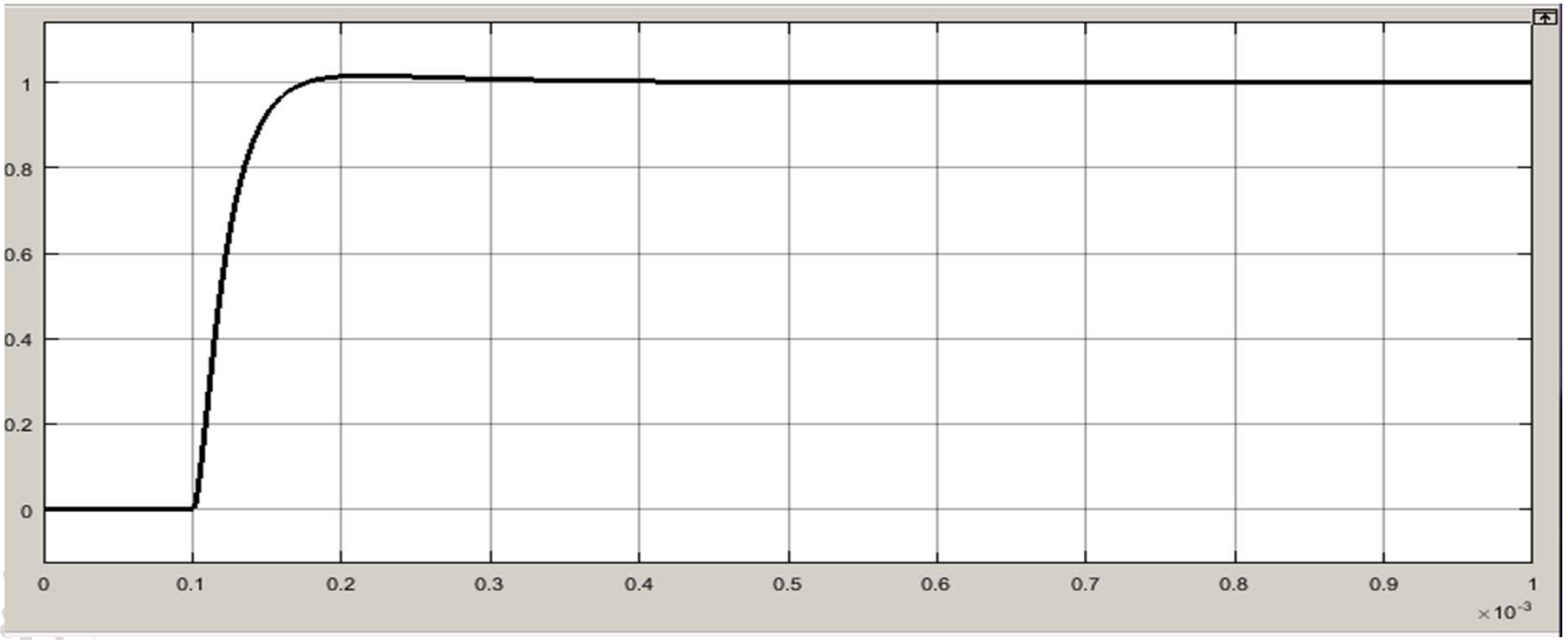
Close Loop system Poles & Zeros

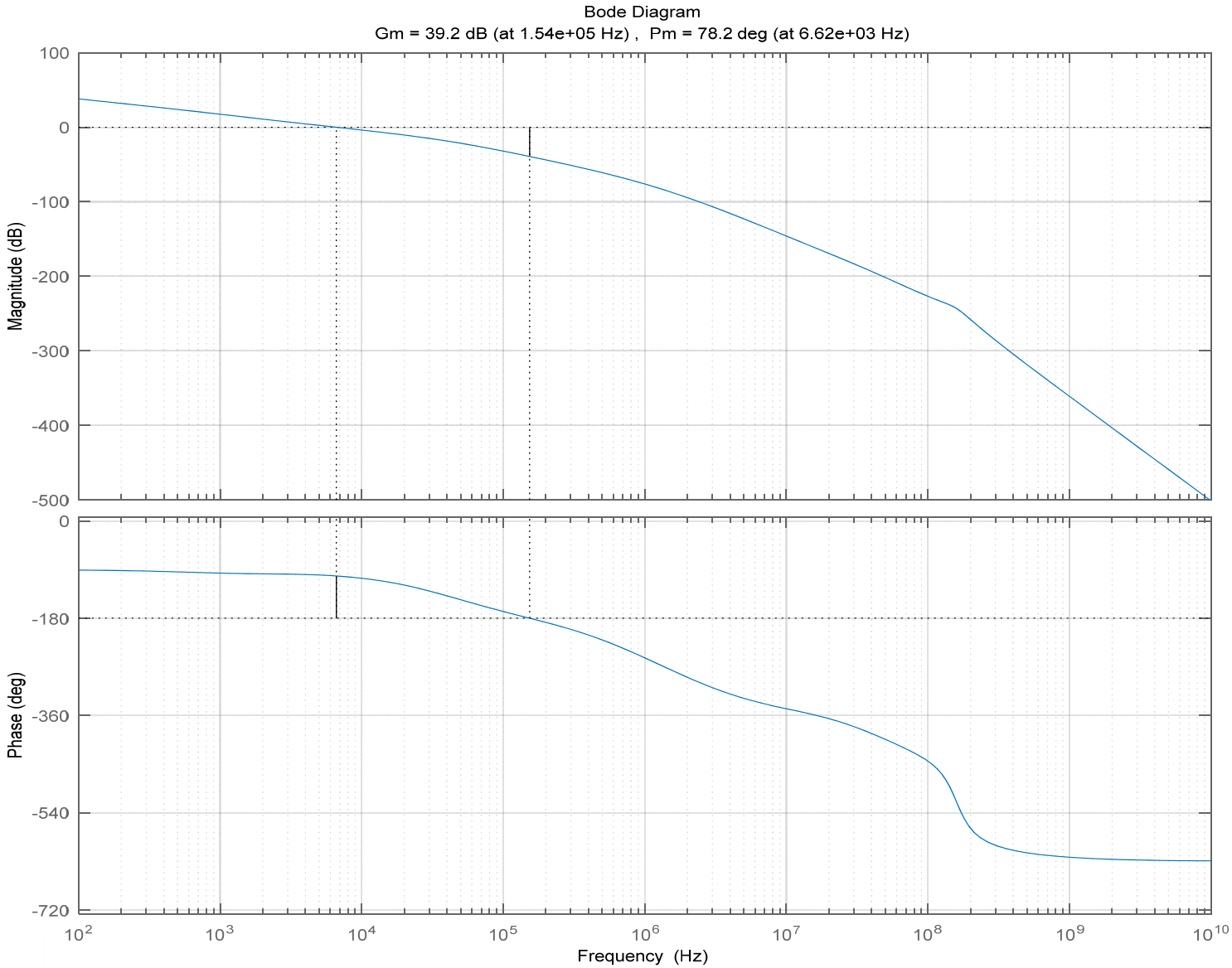
Poles:
-2.3000e+08 + 9.7319e+08i
-2.3000e+08 - 9.7319e+08i
-2.2997e+08
-2.0000e+08
-1.9783e+08
-1.4202e+07
-4.9995e+06
-2.0193e+05
-5.0961e+04
-9.5882e+03

Zeros:
-1.5004e+08
-1.4000e+08
-9.1521e+03

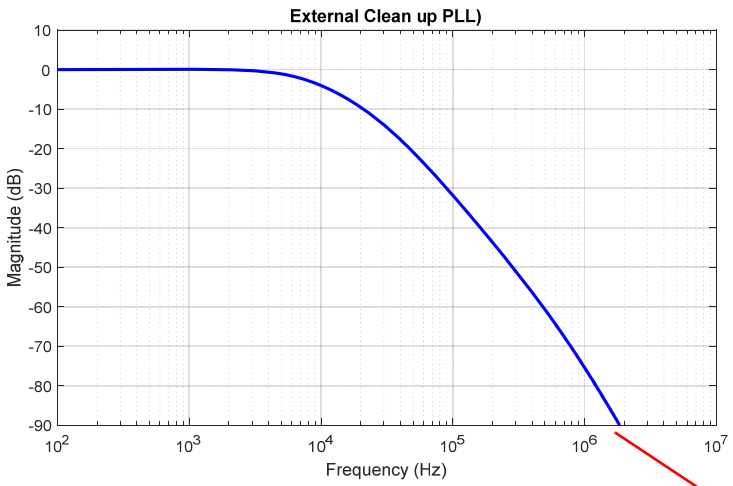


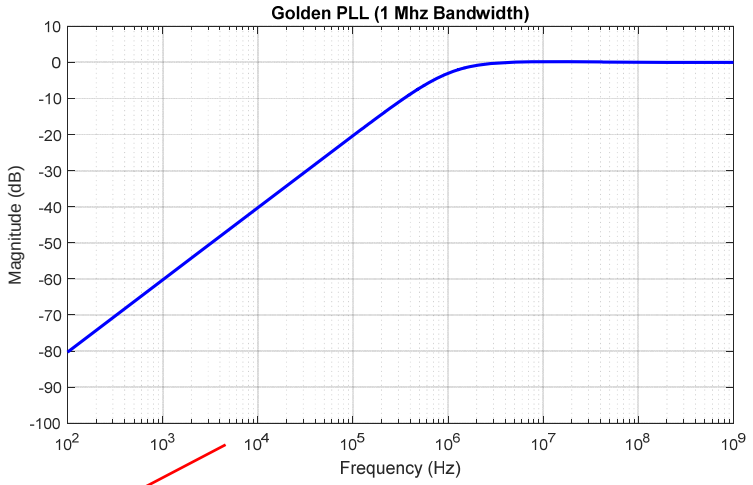

Step
3.316e50s3+9.617e58s2+6.966e66s+6.374e70
s10+1.107e09s9+1.441e18s8+7.249e26s7+1.489e35s6+1.178e43s5+1.874e50s4+6.946e56s3+1.718e62s2+1.267e66s
TF_ol
Scope

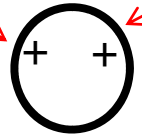

1
0.8
0.6
0.4
0.2
0
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
×10-3

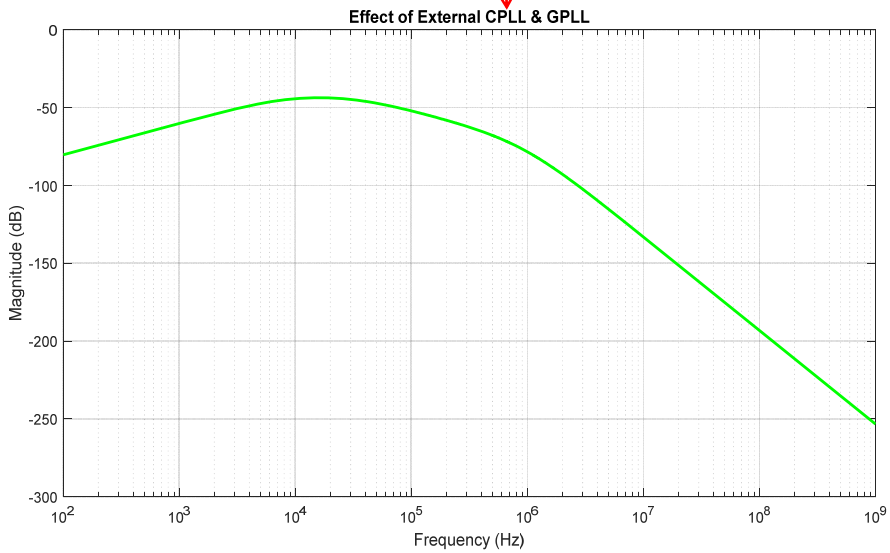

Bode Diagram
Gm = 39.2 dB (at 1.54e+05 Hz) , Pm = 78.2 deg (at 6.62e+03 Hz)
Magnitude (dB)
100
0
-100
-200
-300
-400
-500
Phase (deg)
0
-180
-360
-540
-720
10^2
10^3
10^4
10^5
10^6
10^7
10^8
10^9
10^{10}
Frequency (Hz)

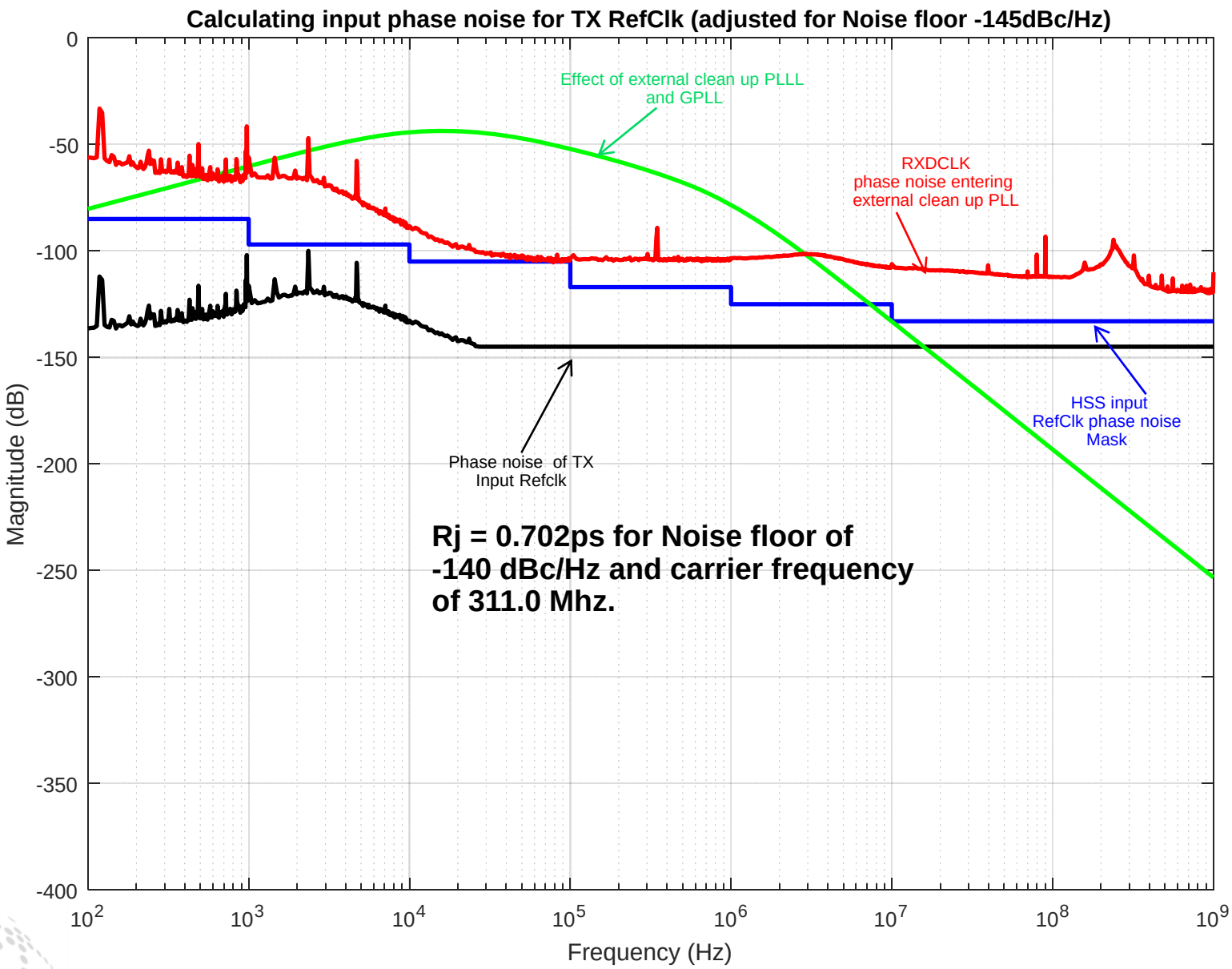
Phase noise analysis of recovered Clock


External Clean up PLL)
Magnitude (dB)
Frequency (Hz)


Golden PLL (1 Mhz Bandwidth)
Magnitude (dB)
Frequency (Hz)

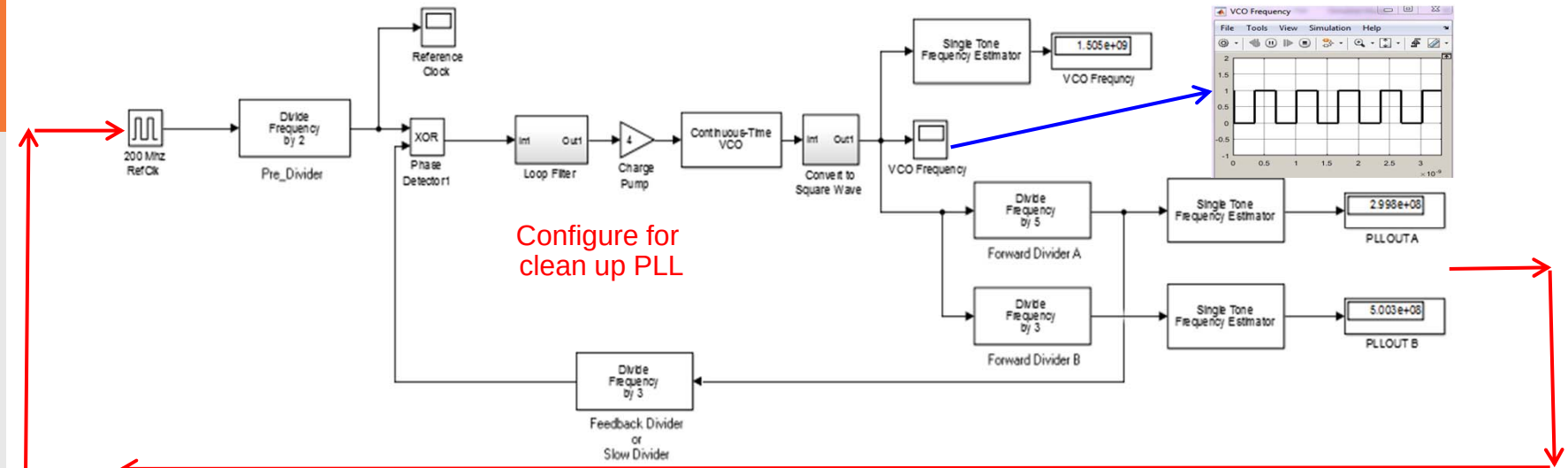

+
+


Effect of External CPLL & GPLL
Magnitude (dB)
Frequency (Hz)


Calculating input phase noise for TX RefClk (adjusted for Noise floor -145dBc/Hz)
Effect of external clean up PLLL and GPLL
RXDCLK phase noise entering external clean up PLL
HSS input RefClk phase noise Mask
Phase noise of TX Input Refclk
Rj = 0.702ps for Noise floor of -140 dBc/Hz and carrier frequency of 311.0 Mhz.
Magnitude (dB)
Frequency (Hz)
0
-50
-100
-150
-200
-250
-300
-350
-400
10^2
10^3
10^4
10^5
10^6
10^7
10^8
10^9

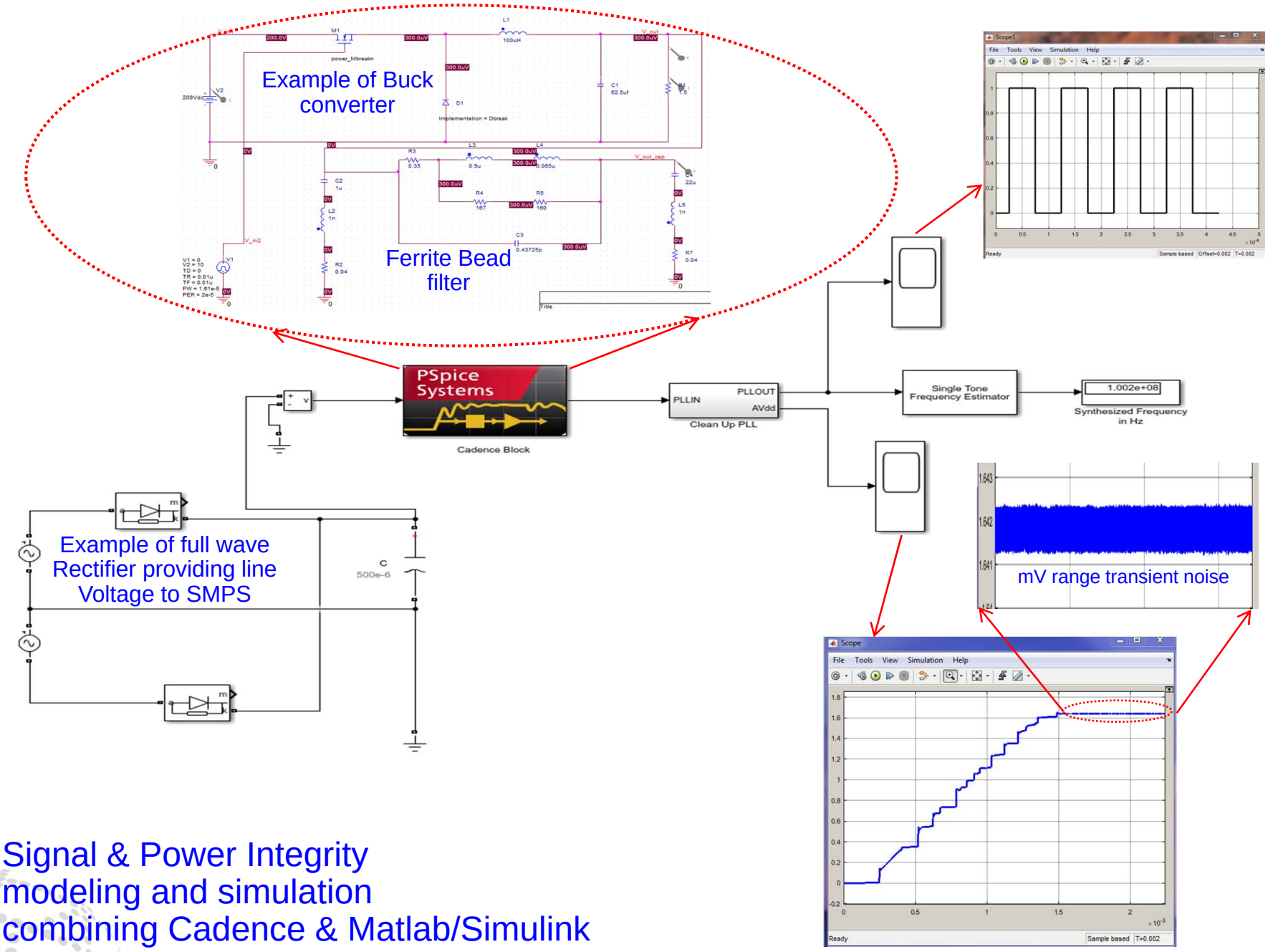
Backup Slides

Possible Methodology for time Domain analysis of closed loop (Under development)



Configure for Tx PLL

Configure for RX/CDR



Signal & Power Integrity modeling and simulation combining Cadence & Matlab/Simulink