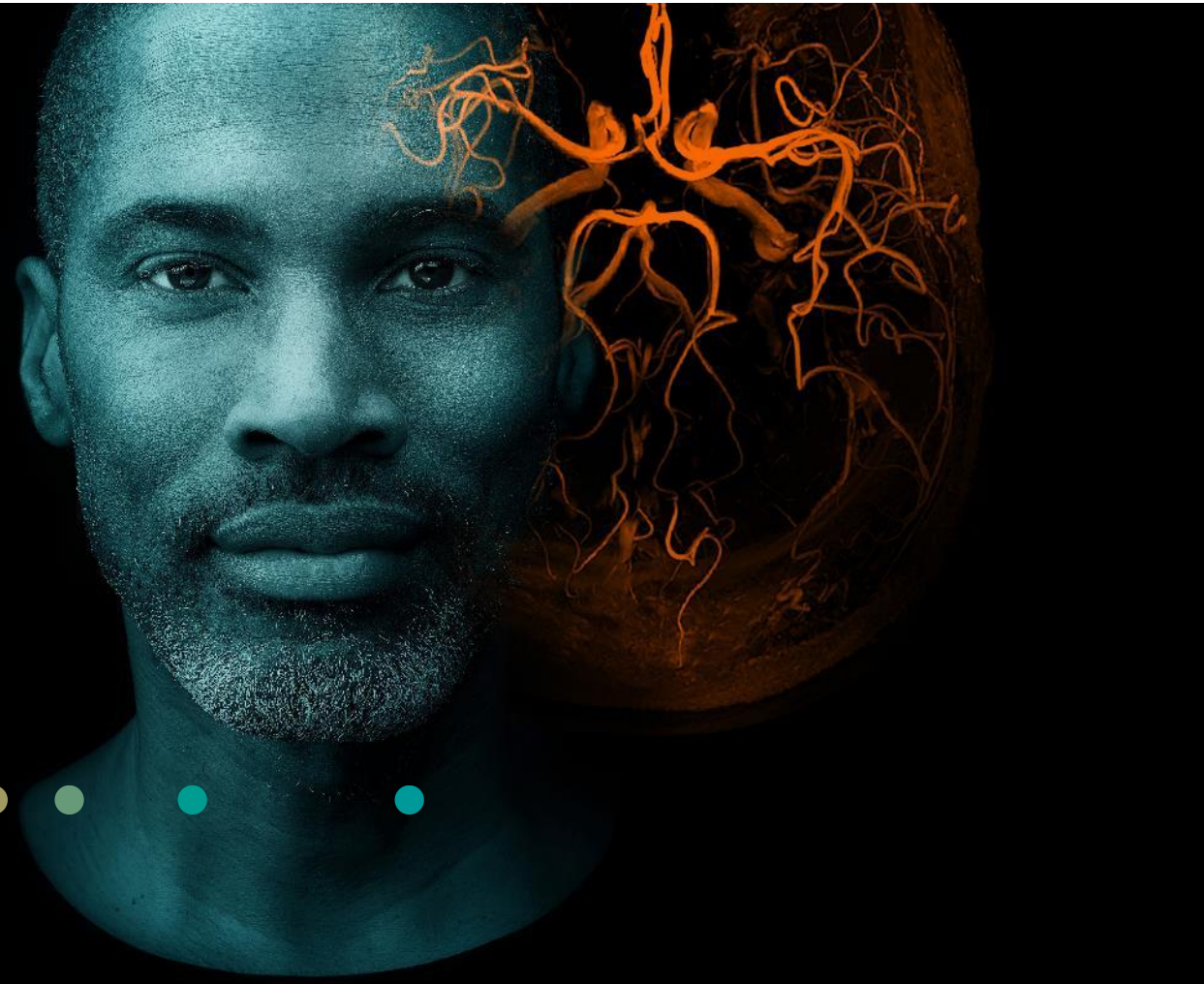
SIEMENS Healthineers

Managing the Complexity of FPGA-Based Rapid Control Prototyping



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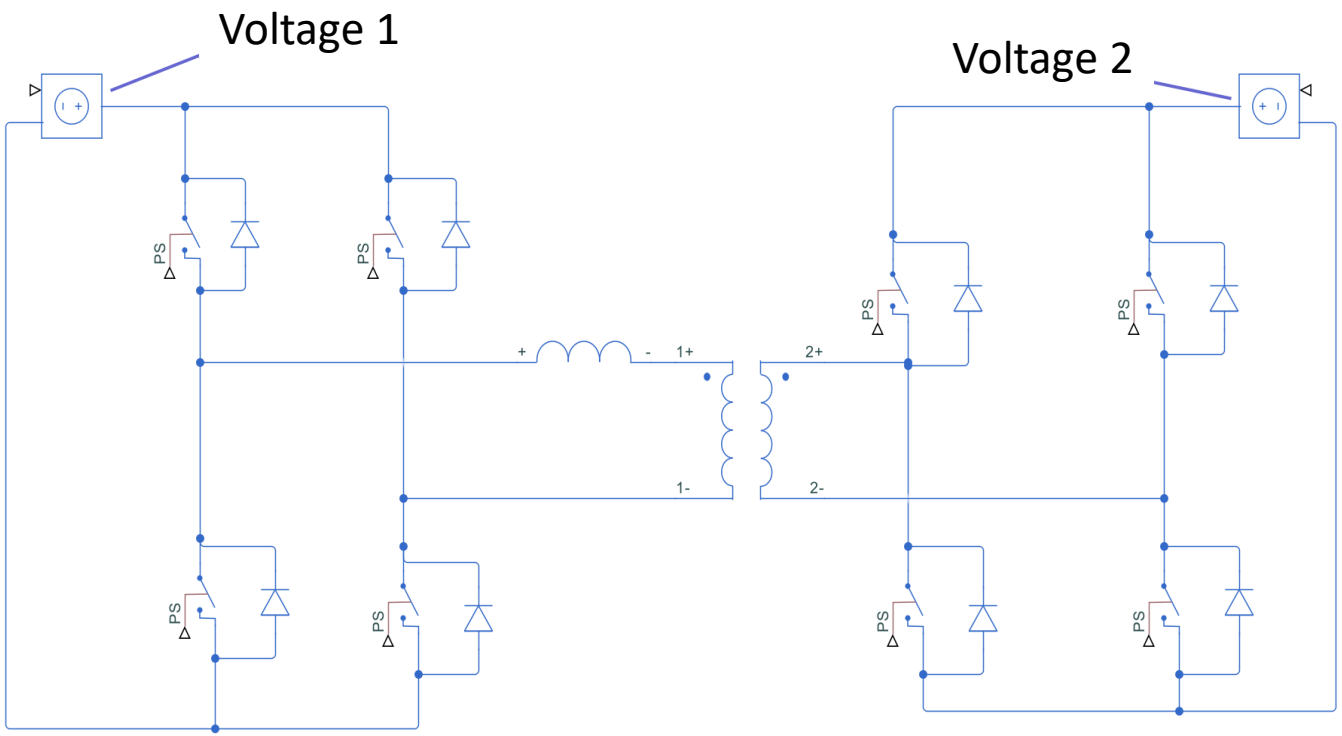
Matlab Expo 2023

DCDC Converter with Dual Active Bridge



DCDC Converter

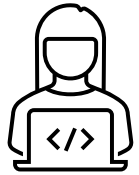
- DCDC Converter is used to transmit electrical power from one component to another component
- Design contains 8 switches that are turned on and off (modulation) by the control unit
- Modulation has impact on energy flow, energy losses and EMC

Developing a Power Electronics Application

I need a control board to run the power application

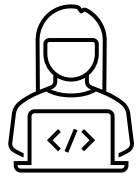
Power Electronics Hardware Developer

I need Firmware to run the control application



Control Electronics Hardware Developer

I need Software to run the firmware application



Firmware Developer

Software Developer

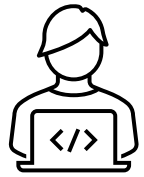
The Hardware developer has to wait for the whole chain, before he can test his prototype

Rapid Control Prototyping

I need a control board to run the power application

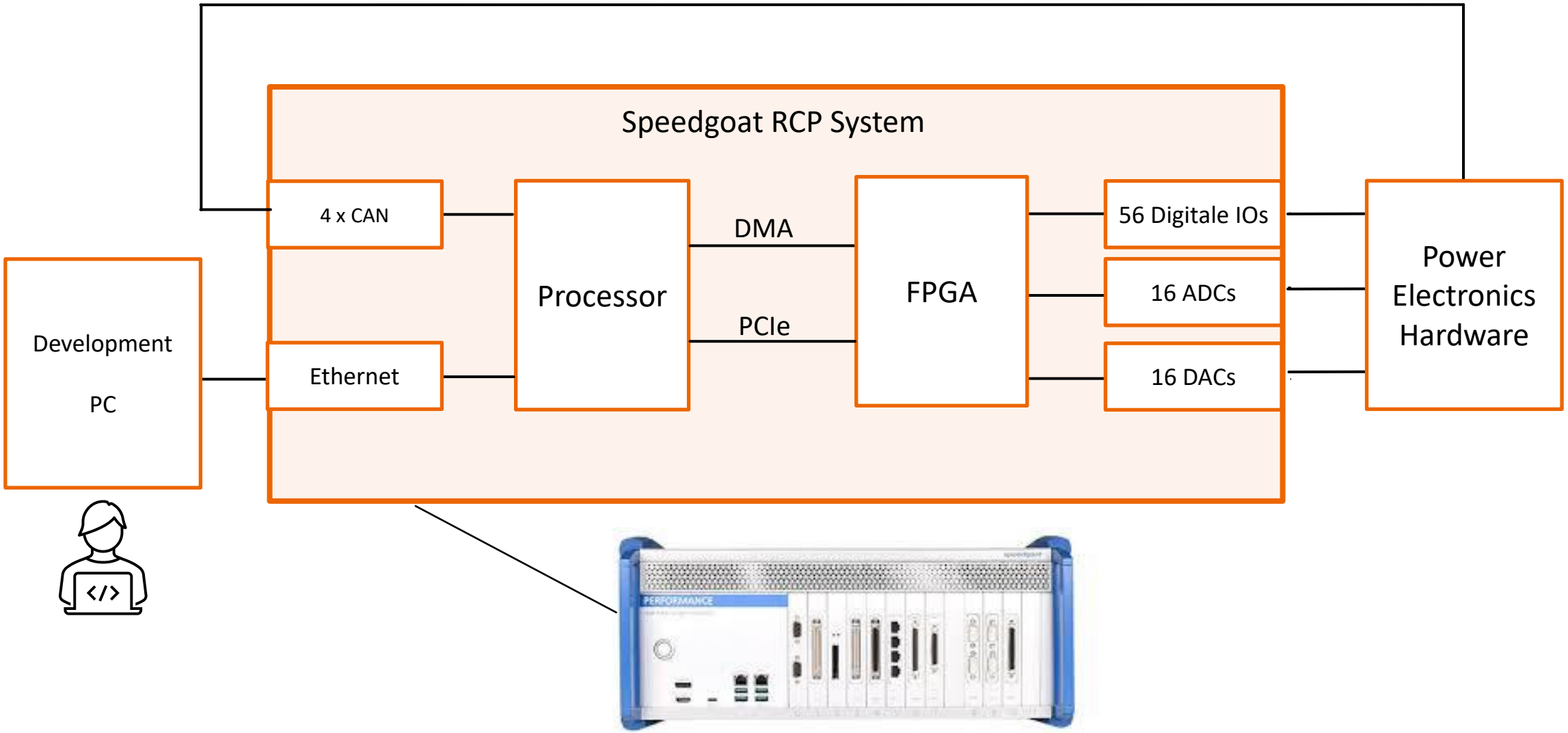
Power Electronics Hardware Developer

Rapid Control Prototyping (RCP) System

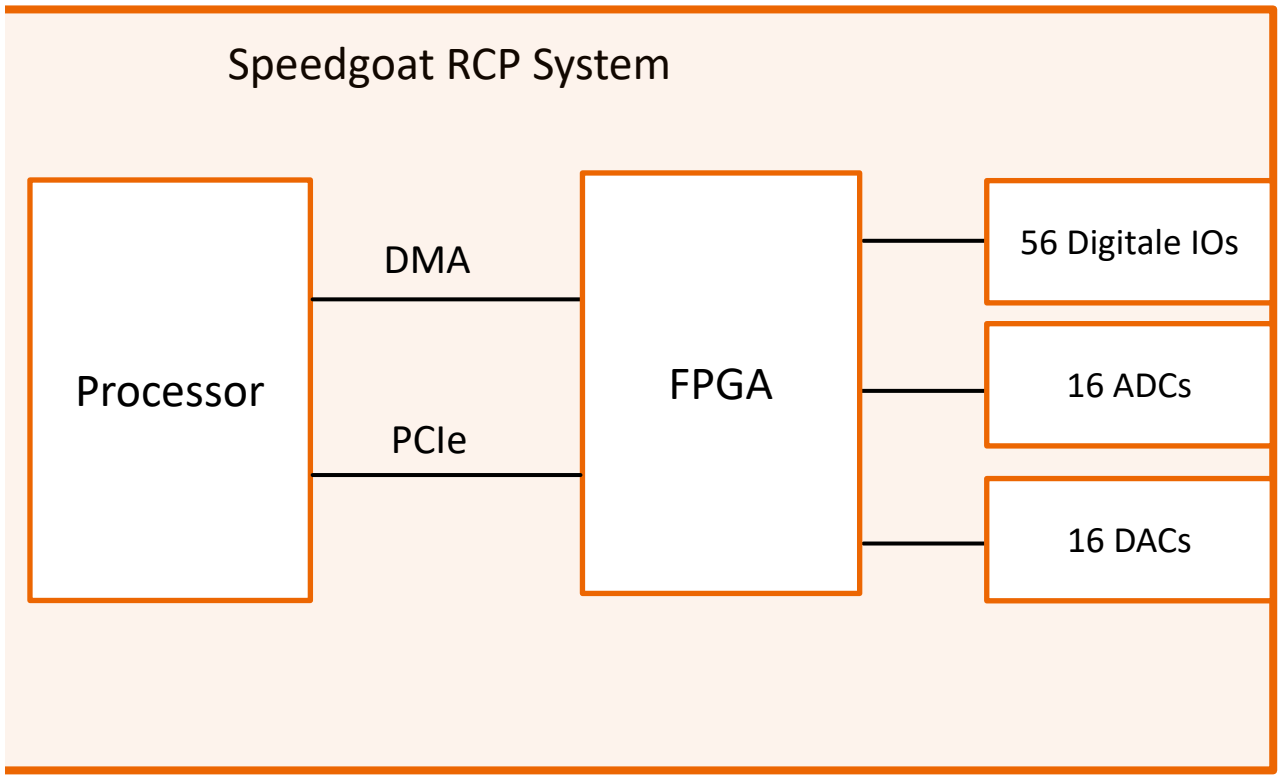


Model Developer

Rapid Control Prototyping



Defining FPGA Interfaces



- All FPGA interfaces are defined in the workflow advisor of the HDL coder
- PCI-express interface
  - multiple channels
  - any data type supported, including Busses
  - CPU-clock-cyles

  → easy to use, but not high performance
- DMA-Interface:
  - 1 channel (requires multiplexing)
  - uint32
  - FPGA-clock-frequency

  → high performance, but not so simple to use

Complexity of FPGA based RCP

Challenges arise from various sources

FPGA specific challenges
- Fixed Point design or
  HDL-coder specific float-implementation
- FPGA-specific timing requirements
- Limited Blocksets
- Limited FPGA Resources
- Long Build durations (> 60 min)

CPU specific challenges
- Limited clock speed

Interface specific challenges
- Limited bandwidth of DMA and PCIe interface
- No Bus-Support for DMA interface

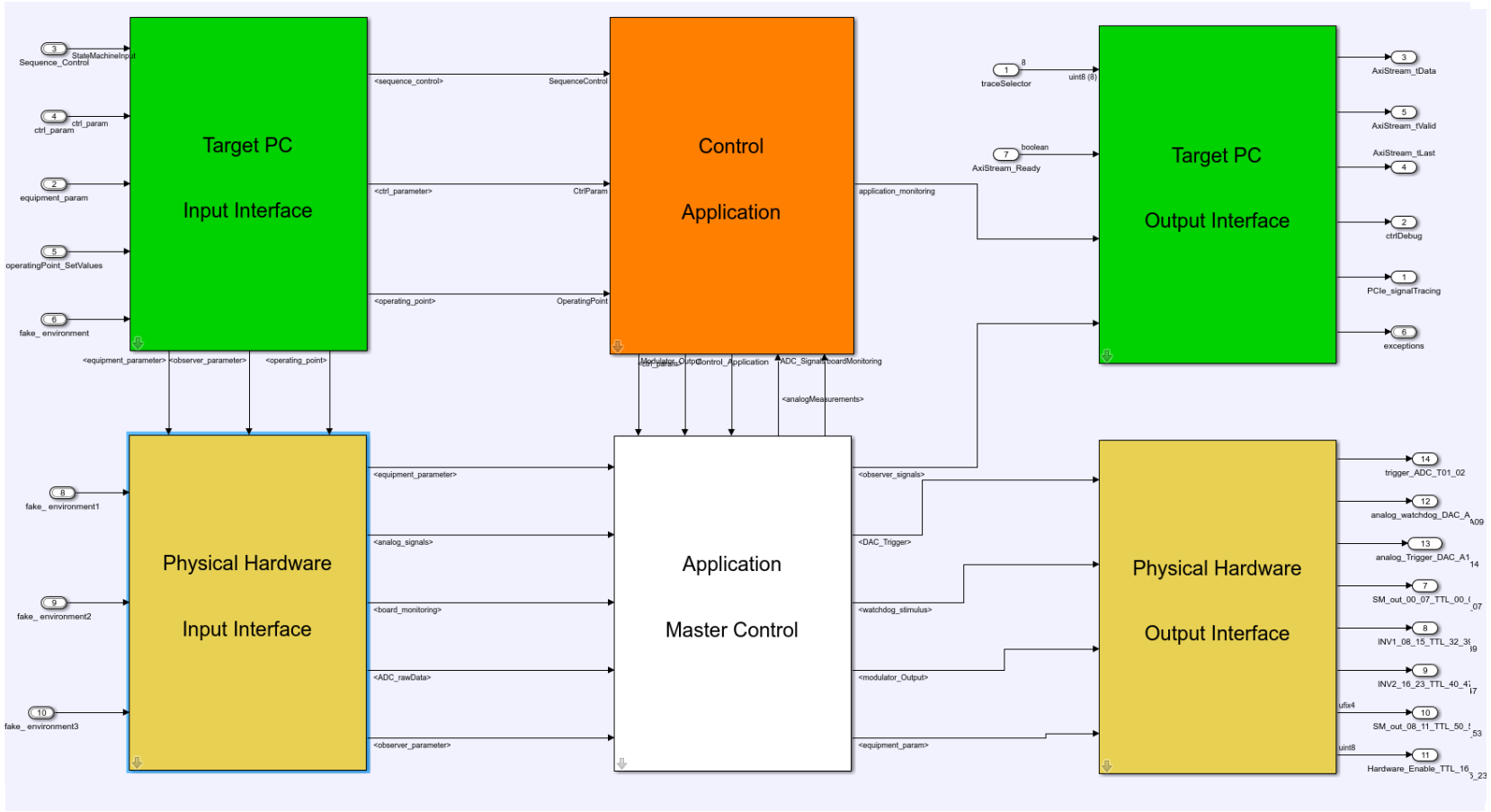
Hardware specific challenges
- Depending on the specific application

EVERYTHING
EVERYWHERE
ALL AT ONCE

None of the challenges is very hard, but there are many of them. Each challenge adds to the complexity of rapid control prototyping.

Model Architecture

Ensure readability and maintainability of model



- Separation of Concerns
- Make use of busses wherever possible
- Ensure Bus-Support for all steps of your build-pipeline
- Clear separation of concerns

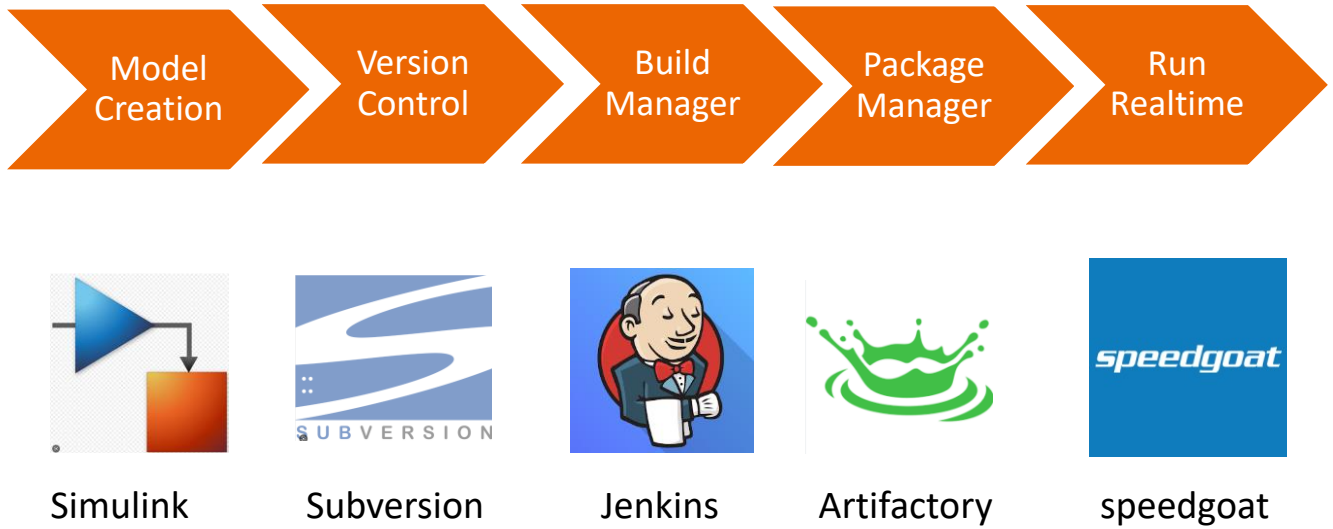
-> Clear separation of
  - Control Application
  - Sofware Abstraction Layer
  - Hardware Abstraction Layer

Build Chain Automation

- Code Generation and FPGA synthesis require approximately 75min (duration depends on model setup, tool setup, and PC speed)

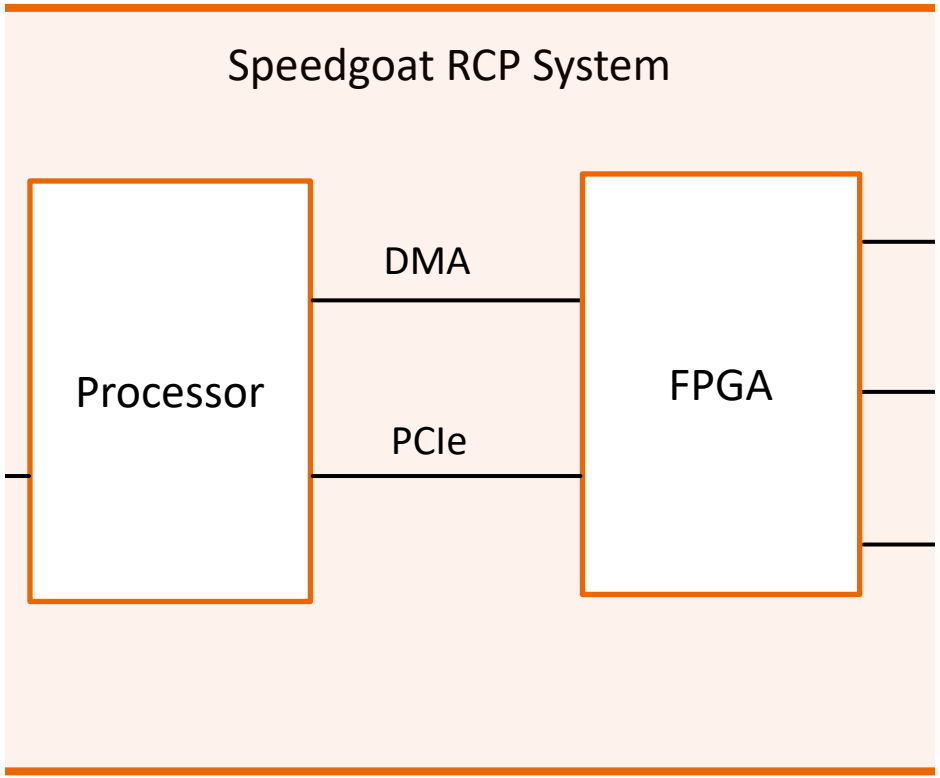
- Make sure that all steps of the build process are completely automated
  - Variant Management
  - VHDL Code Generation
  - Synthesis + Bitstream generation
  - C-Code Generation + Compilation

- Without complete build automation, there will be nothing rapid in Rapid Control Prototyping



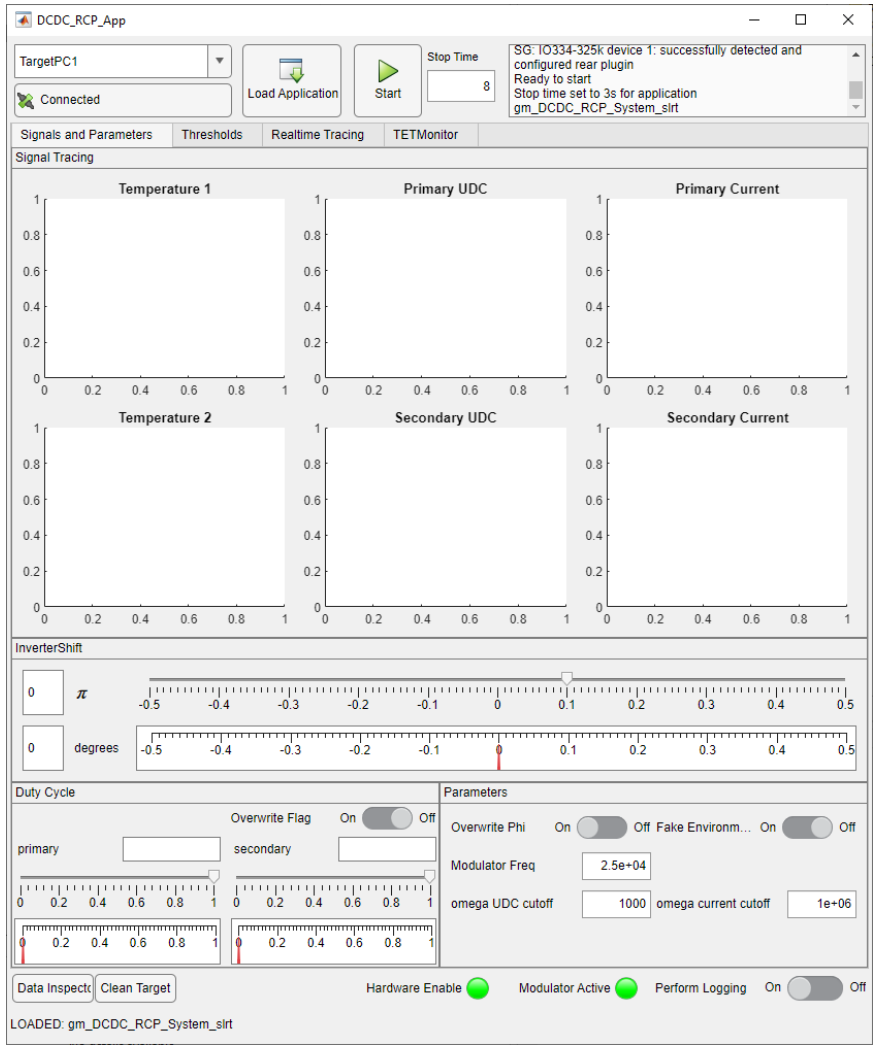
DMA-Utilities

Runtime configuratable tracing in FPGA domain



- DMA allows transfer of 32-bit words @20Ms/s
- Realtime tracing of multiple signals requires multiplexing
- Custom Library for DMA-Support has been created, automating multiplexing of Simulink Busses
- Selection of the tracing signals without FPGA synthesis or C-code generation (runtime configurable)

Life Demo of Realtime Application



Conclusion

- **FPGA based Rapid Control Prototyping has the potential to increase your development speed dramatically**

- **Highest benefits, if you successfully address the challenges of RCP**
  - Maintain a clean Model Architecture
  - Automate all built steps that can be be automated
  - Facilitate a flexible and fast realtime tracing of FPGA based signals